# INTRODUCTION TO HALT - MAKING YOUR PRODUCT ROBUST

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**ABSTRACT**
HALT, Highly Accelerated Life Test, is a process used to discover product weakness and design margins. Used on printed circuit board assemblies (PCBAs) or product modules, it consists of a series of environmental stresses applied to the product in increasing levels of stress, until the product malfunctions or fails. HALT typically utilizes stresses well beyond the product specifications in order to uncover failure modes in the product. By performing failure analyses on the failure modes, and root cause analysis, design improvements can be implemented so as to mitigate or eliminate the failure modes, improving product reliability.

Key words: HALT, HASS, reliability, highly accelerated life test

**INTRODUCTION**
The HALT process is optimally used during the engineering prototype phase to help in the process of product ruggedization. It is primarily a tool to improve product reliability. During the HALT process, product samples are subjected to increasing levels of environmental stress, such as extreme temperatures, temperature cycling and vibration, so as to demonstrate product weaknesses and limitations. Key to the improvement of product reliability is failure analysis and corrective action in response to the failure modes uncovered.

The purpose of this paper is to introduce HALT as a tool for product ruggedization; it may be something you have heard of, but didn't really understand. The goal of this paper is that you may better understand it's purpose, what it does and does not do, and offer suggestions for further investigation.

The real benefits of HALT is that products can be made more reliable as a result of testing in a short period of time; this results in lower warranty costs, as well as happier customers. The HALT process additionally supports the need for rapid time-to-market.

The goal of HALT is to improve the design margin; for example, consider Figure 1 showing product margins and stress, say temperature [1]. The figure shows the product specifications, as well as the Operating Limits and the Destruct Limits; the margin is the temperature difference between, say, the upper operating temperature specification and the Upper Operating Limit (UOL). By implementing design improvements through the HALT process, the margins are increased and the reliability of the product is increased.

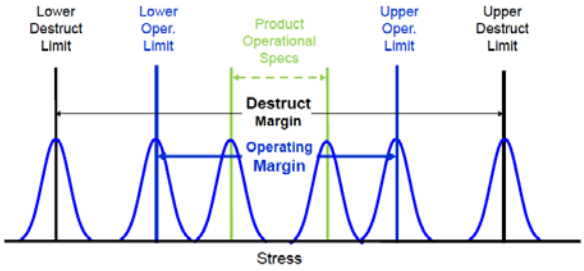


**Figure 1.** Product Margins

**HALT PLANNING AND PREPARATION**
HALT planning typically starts with a new product design plan document, and is discussed in a product reliability or quality plan document; it would include considerations for product warranty costs, product life estimates and goals, and goals for so-called MTBF (Mean Time Between Failure).

The FMEA (Failure Modes Effects Analysis) is a useful process for documenting product failure modes [3]; this is helpful in the HALT planning, as it can be used to plan product test stressors and functional test strategy.

**HALT FIXTURING**
There are three types of fixturing that need consideration.

Electrical - functional test. How to verify that the product is operating correctly.
Mechanical fixturing that supports transferring maximum mechanical energy into the UUT (vibration), and
Thermal - you want a maximum of air flow into and across the electronic portions of the UUT (Unit Under Test) so as to obtain rapid thermal transitions on the UUT.

In some cases, it is desired to monitor test signals inside the product. If desired signal voltages are not readily available through the UUT connectors and software, it may be appropriate to attach voltage sense wiring onto the UUT circuits, and monitor the signals with data loggers. Be careful: this may introduce complex impedance loading into the UUT circuits, interfere with UUT circuit operation. Extreme caution is advised.

There may be specialized electrical cables or components needed for the HALT. Spares should be planned and brought to the HALT test.

**FUNCTIONAL TEST**

You want to perform functional test during HALT so as to verify correct operation of a maximum number of circuit elements: solder joints, connectors, switches, cables, fans, displays, and all of the so-called circuit components, including the fabricated Printed Circuit Board. For complex digital components and circuits, such as a network circuit, you want to have maximum traffic flow. For memory, you want to exercise as many of the memory bits at the maximum rate practical.

It is better if you can borrow the functional test equipment and programs or firmware from other departments, rather than develop them solely for HALT. You may be able to borrow engineering verification equipment, or perhaps manufacturing test equipment. Sometimes there are field service tools that are useful. By borrowing this equipment, you save precious time to develop it, as well as additional costs.

You will need engineering staff present during most of the HALT test. They are key to installing and operating the functional test system, interpreting the results, and to help troubleshoot when failures occur. Many of the failures found during HALT test are due to test system problems (especially if it is based on customer developed firmware or software).

Functional testing will typically consist of 3 types of test routines: simple routines that check functionality of the UUT throughout the HALT process, extensive routines that are run during the dwell time that fully exercise the UUT, and then typically we perform a power cycle process - gracefully shutting down the UUT, and then repowering it.

**HALT TEST STEPS**

There are 5 steps in the HALT process.

In HALT, the product is subjected to progressively higher stress levels, including thermal dwells, rapid temperature cycling (RTC), vibration, and combined rapid temperature transitions and vibration. HALT subjects the product to each of these stresses to the point of failure to assess design robustness and margin above its intended operation. Once the product fails, the failure is fixed, if possible, and then the stress is increased to find the next failure. This process is continued until either the fundamental limit of the technology of the product is reached, or the failure becomes uneconomical to repair. The process will assure that the widest product margins are attained.

The HALT process has been developed on electronic assemblies over the last 30 years or so, and as described here, will uncover defects in the product that are correlated with field failures. Failure modes may be found during the HALT process at stresses beyond those normally encountered in the field, but there are good correlations between those failures found in the HALT process and field failures [3].

During the HALT, the product will be continually monitored for functionality. When a failure occurs, the test diagnostics will log the failure data and all attempts to determine the cause of failure will be made. Depending upon the number of failure modes that are uncovered, the duration of the test could be affected.

There are 5 test steps in the HALT process: Cold Step Stress (CS), Hot Step Stress (HS), Rapid Thermal Cycling (RTC), Vibration Step Stress and Combined Environment.

**COLD STEP STRESS**

The cold temperature step stress will typically begin at 20°C and then the chamber ambient setpoint shall be decreased in 10°C decrements. The dwell time at each thermal step will be 10 minutes. The dwell time will begin after the component temperatures on the product have stabilized (typically 2 minutes). The product will be monitored for functionality throughout the dwell. See Figure 2 for a diagram of the Cold Step Stress test.

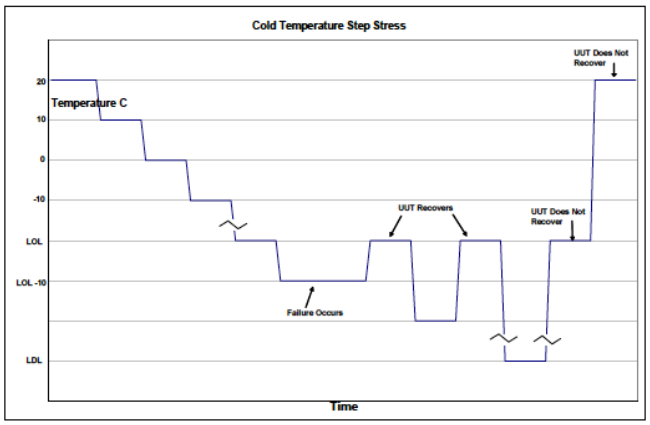


**Figure 2.** Cold Step Stress test

**TEST STEPS - DWELL & FUNCTIONAL TESTING**

Figure 2 shows the setpoints of the chamber temperature. Each dwell is typically 10 minutes, during which time the product temperature stabilizes and then functional testing is conducted on the UUT. In the figure there is a failure at "LOL-10", 10 degrees below the Lower Operating Limit, and then when the temperature is increased 10 degrees, the UUT recovers. Later testing shows a failure at LDL, the Lower Destruct Limit, and when the temperature is raised the product does not recover.

During each dwell time, the UUT would be monitored for functionality. Typically, that functionality would be monitored as described in Table 1.

**Table 1.** Typical functional test sequence during each dwell. Note that test data would be logged continuously with time and date stamp.

| Step Name | Description |
|---|---|
| Temperature Soak | Stabilize temperature |
| Diagnostics - simple | Perform functional test to ensure product is operational; this simple diagnostics test would be running continuously throughout the HALT process, during the ramping up or down, and during dwell. |
| Diagnostics - full | A full diagnostics suite would be performed after temperature stabilization, once during each dwell. |
| Increased Circuit or Signal Stress Test | Increased stress factors would be introduced, during functional test, such as reducing the input supply voltage, pulling of the crystal frequencies, or increased data traffic. |
| Power Cycling Test | Power down the UUT gracefully, and then power it back on and verify that the product goes through its power-up sequence successfully. |

When a failure occurs, the temperature will be returned to the previous level. Once the temperature stabilizes, the functional test will be repeated to verify the product's functionality has not been permanently degraded (a destruct failure). The lowest temperature at which the product is functional is defined as the Lower Operating Limit (LOL).

Assuming sufficient samples are available, the test temperature will be reduced further to discover the destruct limit - the temperature at which the UUT fails, and does not recover.

Key to the process is that whenever a problem occurs, engineering staff is on hand to perform root cause failure analysis. Design changes can be implemented on the spot, so as to reduce or eliminate the failure mode, or to at least mitigate it so that testing can be continued with increasing stress levels (cold temperatures decreased further, in this case). Testing would continue until the limits of technology or practical limits are encountered, which is typically well beyond the stresses found in normal operation.

## HOT STEP STRESS

The hot temperature step stress will begin at 20°C and then shall be increased in 10°C increments. The dwell time at each thermal step will be 10 minutes. The dwell time will begin after the component temperatures on the product have stabilized. The product will be monitored for functionality throughout the dwell. See Figure 3 for a diagram of the process. See Table 1 for the functional tests to be performed at each temperature step stress.

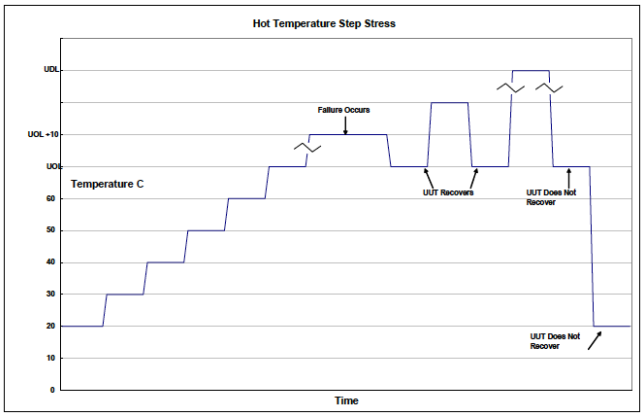


**Figure 3.** Hot Step Stress Process

As with the Cold Step Stress test, the temperature testing would continue, with increasing temperature setpoints, until the Upper Operating Limit and possibly the Upper Destruct Limits are found. Again, key to improving product reliability is the failure analysis and design improvements for each problem found.

## RAPID TEMPERATURE CYCLING (RTC)

Using the temperature operating limits determined during the cold and hot thermal step stress processes, the product will be subjected to 5 thermal cycles. The dwell time at each extreme will be a minimum of five minutes and the thermal transition rate will be set to the chamber maximum (approximately 40 to 60°C per minute, depending on product size and weight). The primary stress of this test is the temperature transition itself, looking for issues related to the differences in thermal coefficients of expansion and contraction on the product. The product will be monitored throughout the rapid thermal transition process. See Figure 4.

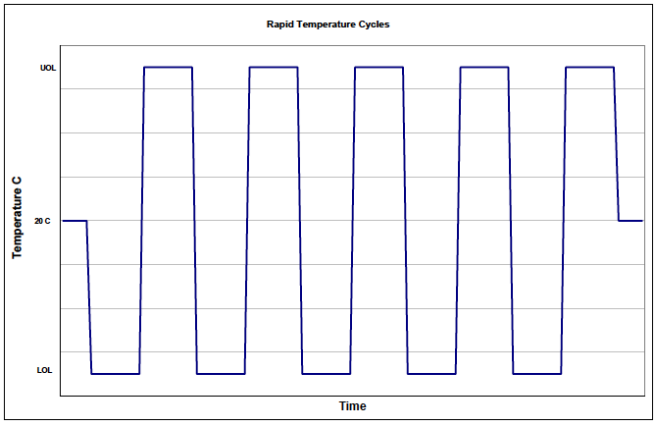


**Figure 4.** Rapid Temperature Cycling

Note that the initial step starts out going cold. This means that the final ramp will be cooling from a hot temperature, so that when you finish, the chamber can be opened up without condensation occurring.

Product Fixturing should be designed so that a high volume of air is blown onto the electronic assemblies with the

maximum cooling and heating ramp rates; thermocouples should monitor the temperatures of the sensitive electronics (rather than only the chamber air temperature).

## VIBRATION STEP STRESS

The vibration step stress will begin at a set point of 5 Grms and will be increased in 5 Grms increments until a failure occurs or the chamber maximum is reached. The dwell time at each vibration step will be 10 minutes. The product will be monitored for functionality throughout the dwell.

When the first failure occurs, the vibration will be returned to the previous level. Once the vibration stabilizes, the functional test will be repeated to verify the product's functionality has not been permanently degraded (destruct failure). The highest vibration at which the product is functional is defined as the Vibration Operating Limit (VOL). See Figure 5. Note however that most failures that occur during vibration are destructive; products rarely experience vibration failures and fully recover at lower levels of vibration.

At each set point after the 25 Grms level, the vibration will be decreased to 5 Grms to determine if a failure occurred that could not be detected at the higher vibration levels. If no failures are detected during this "tickle vibration", the vibration will be increased to the next level.

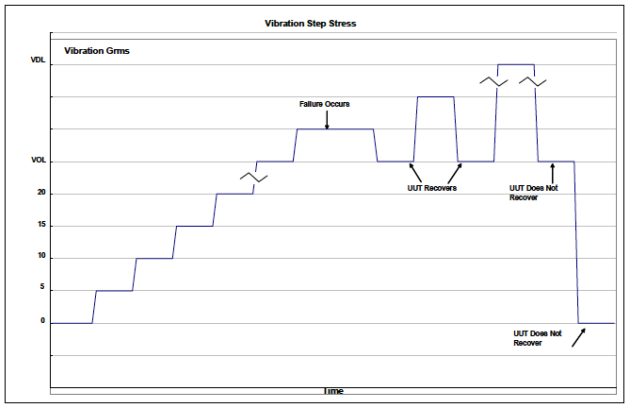


**Figure 5.** Vibration Step Stress ("tickle" step not shown)

Product fixturing should be designed so as to maximize the amount of vibrational energy transmitted into the electron portion of the UUT. Thus, metal fixture brackets are preferred over plastic ones (such the product case for a consumer product). Also, it is desirable to design the fixturing to avoid large resonances - such as would occur if a Printed Circuit board assembly had fixture brackets at the 4 corners.

## COMBINED ENVIRONMENT TESTING

The combined environment process subjects the product to rapid temperature cycling and vibration step stress testing simultaneously. Using the temperature operating limits determined during the thermal step stress process, the product will be subjected to 5 rapid temperature cycles combined with vibration. The vibration level during the first cycle will start at 20% of the Vibration Operating Limit (VOL). The vibration level will be increased in 20% increments for each additional thermal cycle. The dwell time at each temperature extreme will be a minimum of 10 minutes with the thermal ramp rate set to the chamber maximum. The product will be monitored for functionality throughout the test.

If a failure has not occurred upon completion of 5 combined environment cycles, another five cycles will be performed using the following criteria. The vibration level will be constant at the VOL, and the upper and lower temperatures will be expanded by 5°C at the beginning of each thermal cycle. The dwell time at each extreme will be a minimum of 10 minutes and the thermal ramp rate will be set to the chamber maximum. If the product stops operating at either thermal extreme during the dwell, then at the end of the dwell, the temperature shall be brought back to the operating limit, assuring that the product starts operating again before ramping to the next level. See Figure 6. Testing will continue until the UUT has failed.

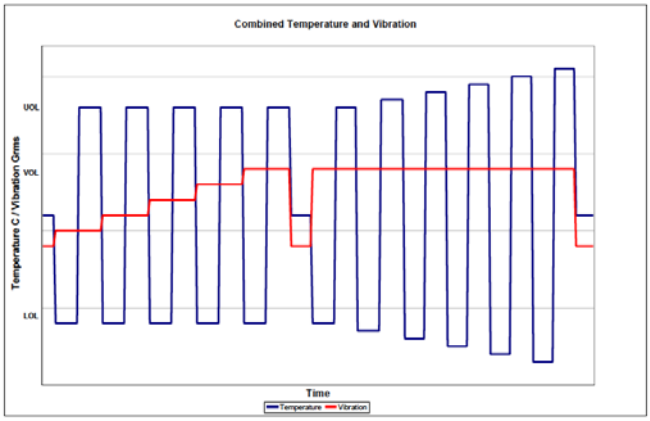


**Figure 6.** Combined Environment Test

## TYPICAL FAILURES FOUND IN THE HALT PROCESS

Table 2 lists some of the typical failures found during the HALT process. While most of these are hardware or mechanical in nature, a number of software or firmware problems show up during the HALT process.

**Table 2.** Typical HALT Failures

| Failure Mode |
|---|
| Broken lead |
| Screws back out |
| Socket failures |
| Connector backs out |
| Tolerance issue |
| Card backs out |
| Shorted component |
| Broken component |
| RTV applied incorrectly |
| Potentiometer turns |
| Plastic cracks at stress point |
| Intermittent component |
| Failed component |
| Connectors wearing |
| Connector making intermittent contact |
| Connector breaks from board |
| Broken trace |
| Product Software / Firmware failures |
| Solder Joint intermittent or failing |

## RESULTS OF HALT

A study was conducted on 47 products tested with the HALT process [3]. Figure 7 shows the distribution of failures found during each step of the HALT process. Note that the maximum number of failures occurred during the Vibration Step Stress testing. However, more significantly, note that 20% of the failures were found during the Combined Environment testing; these failures would not have been uncovered if only temperature and vibration testing alone was performed.

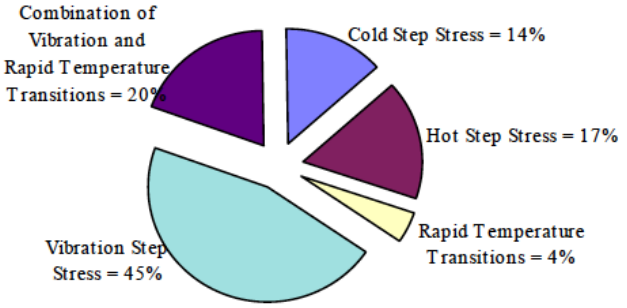


**Figure 7.** Breakdown of HALT Failures by HALT Step

## BARRIERS TO A SUCCESSFUL HALT

A common barrier to a successful HALT is in not understanding the need to stress the product to levels well beyond the product specification. There is correlation between the failures found in the HALT process and those found in the field, as long as the failure modes are related. However, sometimes it is tempting to restrict the HALT stress levels so that the product does not fail. This does not result in discovery of failure modes, and thus, there is less opportunity to improve the product reliability.

Another barrier to a successful HALT is if there is a lack of failure analysis and root cause determination. Without understanding of the failure modes, HALT becomes a sort of characterization test, perhaps useful in identifying operating limits or destruct limits; this in itself does not improve the reliability of the product.

## HASS - HIGHLY ACCELERATED STRESS SCREENING

HASS is a manufacturing stress screening process, based on the results of HALT. HASS is non-destructive, and is primarily aimed at screening out manufacturing defects and weak components. It is not aimed at detecting product design defects, although they may in fact be discovered during the HASS process. Discussion of HASS and HASA (Highly Accelerated Stress Audit) is given in the literature [1].

## CONCLUSIONS

A general discussion of the HALT process has been given to help introduce the reader to the topic.

For the person unfamiliar with HALT, this material should give them a better understanding of what HALT is, when it is appropriate to use, how to get it done and what is involved, as well as an understanding of some of the subtleties and barriers to successful HALT.

A next step would be to select a product that is in the engineering prototype phase, and perform the HALT process on it [1,4].

## ACKNOWLEDGEMENTS

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